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DRAWING

The Examiner has required Applicants to label figure 1 as prior art. In making this requirement, the Examiner appears to misinterpret certain text in the specification. The cited portion of the text indicates that this is a "common" framework. This text does not mean that the figure is known, necessarily. This text means that the scheme illustrated in the figure can be used in common by all existing broadcast standards. The undersigned is not willing to concede that this figure is prior art without more evidence.

SECTION 112 REJECTION

Applicants respectfully disagree that claim 6 is not supported in the specification. Page 2, lines 2-3 clearly support this recitation. Nevertheless, Applicants are adding an additional figure herein to satisfy the drawing requirements of the regulations. Text supporting the new drawing is also added. Applicants respectfully submit that no new matter has been added, because the new text & figure only track the language of the existing claim.

The language of claim 6 has been changed to make it more in keeping with traditional US claim format. Applicants respectfully submit that the scope of the claim has not been changed.

ART REJECTIONS

The art rejections are respectfully traversed.

Since the references are long and complex, Applicants have read the portions of them pointed to by the Examiner. Applicants do not pretend to have read each and every word of the references.

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Claim 1 recites inter alia

- a set of co-processors including at least 3 clusters of programmable co-processors for executing the functions of a digital front-end block (DFE), a channel correction block (CHN) and a forward error correction block (FEC), ***respectively***, [emphasis added]

The word "respectively" is emphasized here, because it means something that the Examiner appears possibly not to have appreciated. In other words, there is a cluster of co-processors for the DFE, a cluster of co-processors for the CHN, and a cluster of co-processors for the FEC.

Uchida's figures 6a and 6b are cited against this recitation. These figures show three front end devices — which the Examiner perhaps considers to be analogous to Applicants' DFE — with a common processor. Applicants do not understand how these front end devices are relevant to claim 1, however, because Applicants do not see that they are programmable as recited in claim 1 — nor has the Examiner indicated where Uchida teaches that they are programmable. It appears instead that there is a separate, non-programmable front end device for each format. Moreover, Applicants are not finding where the Examiner is reading the claim recitations relating to the CHN & FEC on Uchida at all.

In an attempt to correct at least the absence of the CHN in Uchida, the Examiner cites Stott. But Stott, so far as Applicants can tell, relates to ASIC devices that are also not programmable. Nor has the Examiner indicated where Stott teaches that this device is programmable. Accordingly, with respect to the clusters of co-processors recited by Applicants, Uchida and Stott appear to be similarly deficient in not showing *programmable* co-processors.

Moreover, Applicants are not seeing where the Examiner has read the recited forward error correction block on any of the references.

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Claim 1 further recites

- a general purpose processor (DSP) for managing control, synchronization and configuration of the channel decoder,

The Examiner turns to the DSP of Garde with respect to the recited general purpose processor. The Examiner points to this DSP as optimizing performance for applications; however, so far as Applicants can tell these applications are occurring within the DSP. Applicants are not seeing — nor has the Examiner pointed to — where Garde teaches or suggests that its DSP is for managing control, synchronization and control of a decoder having multiple co-processors. It does not appear that this DSP is portable to Applicant's environment.

It should be noted that the use of the abbreviation "DSP" in both the present application and Garde does not mean that the similarly labeled digital signal processors are performing the same functions at all.

Accordingly, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case of obviousness against claim 1.

Independent claims 4 and 6 are analogous to claim 1 in that they recite the steps of

- base-band demodulation,
- channel correction and
- forward error correction of the received signal.

Again the Examiner has not read forward error correction against any of the references. The claim further recites that like claim 1 that each step is performed by a cluster of *programmable* co-processors. Again the Examiner has not demonstrated where any of the devices in the prior art

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are programmable as recited by Applicants. Accordingly, Applicants respectfully submit that the Examiner has failed to make a prima facie case of obviousness against claims 4-6.

New claims

Claims 4-6 do not include the word "respectively", unlike claim 1, but this limitation has been added to new dependent claims 8-10. These new claims accordingly distinguish even more clearly over the reference than claims 4-6 do.

New claim 11 is also somewhat analogous to claim 1 with respect to the arguments given for claim 1 above, except that the limitations are all set out more positively rather than inferentially and in outline format. Applicants hope that the Examiner will better understand the limitations in this format. New claim 11 may be slightly broader than the other claims, because of the repetitions of the phrase "at least one." Claim 11 also adds the limitations that each cluster is adaptable to all the formats. Applicants respectfully submit that this last limitation clearly distinguishes patentably over the references.

New claims 7-10 add a similar limitation to the other independent claims.

Applicants accordingly respectfully submit that the new claims distinguish patentably over the reference.

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Claim 2

With this rejection, the Examiner is up to 4 references that he is combining to allegedly find the claim obvious. The number of references in and of itself militates in favor of a conclusion of non-obviousness.

Moreover, Applicants respectfully submit that the Examiner has used Applicants' claims as a map for creating an improper hindsight reconstruction of the invention by picking unrelated pieces out of the references without finding any motivation in the references themselves for making such combinations. The motivation instead comes from Applicants' disclosure and Applicants' claims.

Furthermore, Applicants are unable to find that the Examiner has shown any of the pieces of the prior art references cited against the new recitations of claim 2 to be co-processors as recited in claim 2.

Applicants accordingly respectfully submit that the Examiner has failed to make a *prima facie* case of obviousness against claim 2.

Claim 5

With respect to the recitations of claim 5, the Examiner adds a citation to Sarfati again using four references in an improper hindsight reconstruction.

Moreover, Applicants respectfully submit that the Examiner mischaracterizes Sarfati. Sarfati apparently relates to downloading an executable application. However, Applicants are

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unable to find that this downloaded executable relates to programming decoding functions as recited by Applicants.

The Examiner's other rejections and/or points of argument not addressed would appear to be moot in view of the foregoing. Nevertheless, Applicants reserve the right to respond to those rejections and arguments and to advance additional arguments at a later date.

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Applicants respectfully submit that they have answered each issue raised by the Examiner and that the application is accordingly in condition for allowance. Allowance is therefore respectfully requested.

CERTIFICATE OF MAILING

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Respectfully submitted,

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March 23, 2004